REMARKS

The Examiner is thanked for the thorough review and consideration of the present application. The final Office Action dated July 2, 2003 has been received and its content carefully reviewed.

By this Response, Applicant has amended claims 1, 6 and 10 to clarify the subject matter of the present invention. No new matter has been added. Claims 1-16 are pending in the application. Reconsideration and withdrawal of the rejection in view of the above amendments and the following remarks are requested.

In the Office Action, claims 1, 2 and 6-16 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,335,770, issued to Komatsu. Applicant traverses the rejection because Komatsu fails to teach or suggest each of the features recited in the claims of the present application. In particular, Komatsu fails to teach or suggest an in-plane switching mode liquid crystal display device having, among other features, "a plurality of common voltage lines, being provided in such a manner to cross the plurality of gate links, for applying a common voltage to a liquid crystal at the outer area of the thin film transistor array to reduce a gate voltage at the plurality of gate links", as recited in amended independent claim 1; "a plurality of common voltage lines parallel to the gate lines and crossing the gate links, wherein the plurality of common voltage lines are configured to apply a common voltage to a liquid crystal at the area outside the thin film transistor array to reduce a gate voltage at the plurality of gate links", as recited in amended independent claim 6; and "a plurality of common lines extending between the signal pads and the thin film transistor array, wherein the plurality of common lines are configured to apply a common voltage to a liquid crystal at the area outside the thin film transistor array to reduce a gate voltage at the signal pad area", as recited in amended independent claim 10.

Applicant notes that Komatsu discloses gate and data bus lines 101 and 102 which are connected to gate and data driving circuits through gate and data pads 151 and 155 respectively. Also, a common bus line 103 is grounded through a common pad 157. (See, col. 5, lines 40-47). However, Applicant respectfully submits Komatsu fails to teach or suggest applying a common voltage to a liquid crystal at the outer area of the thin film transistor array to reduce a gate

voltage as recited in claims 1, 6 and 10. As such, Komatsu fails to anticipate the claims of the present application. Reconsideration and withdrawal of the rejection of claims 1, 2 and 6-16 are requested.

In the Office Action, claims 1-16 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,456,350, issued to Ashizawa et al (hereafter "Ashizawa"). Additionally, claims 3-5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ashizawa. Applicant traverses the rejections because Ashizawa fails to teach or suggest each of the combined features recited in the claims of the present application. For example, Ashizawa fails to teach or suggest an in-plane switching mode liquid crystal display device having:

> "a plurality of common voltage lines, being provided in such a manner to cross the plurality of gate links, for applying a common voltage to a liquid crystal at the outer area of the thin film transistor to reduce a gate voltage at the plurality of gate links", as recited in amended independent claim 1;
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> "a plurality of common voltage lines parallel to the gate lines and crossing the gate links, wherein the plurality of common voltage lines are configured to apply a common voltage to a liquid crystal at the area outside the thin film transistor array to reduce a gate voltage at the plurality of gate links", as recited in amended independent claim 6; and
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> "a plurality of common voltage lines parallel to the gate lines and crossing the gate links, wherein the plurality of common voltage lines are configured to apply a common voltage to a liquid crystal at the area outside the thin film transistor array to reduce a gate voltage at the plurality of gate links", as recited in amended independent claim 10.

Applicant notes that Ashizawa discloses a plurality of common lines in various configurations as described, for example, in figures 6 and 7. However, Applicant respectfully submits Ashizawa fails to teach or suggest common voltage lines configured to apply a common voltage to a liquid crystal at the outer area of the thin film transistor array to reduce a gate voltage at the plurality of gate links, as recited in claims 1 and 6; and a plurality of common lines extending between the signal pads and the thin film transistor, wherein the common lines are configured to apply a common voltage to a liquid crystal at the area outside the thin film transistor array to reduce a gate voltage at the signal pad area, as recited in claim 10.

Because Ashizawa fails to teach or suggest at least each of the features recited in independent claims 1, 6 and 10, Ashizawa fails to anticipate claim 1 and its dependent claims 2-5, independent claim 6 and its dependent claims 7-9, and independent claim 10 and its dependent claims 11-16. Reconsideration and withdrawal of the rejection of claims 1-16 are requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed

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Respectfully submitted,

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